SMC-02-353

December 10, 2003

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/661,746 09/12/03

Chia-Ta Hsieh

A METHOD TO SHRINK CELL SIZE IN A SPLIT GATE FLASH

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 19, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 12/19/03

U.S. Patent 5,915,178 to Chiang et al., "Method for Improving the Endurance of Split Gate Flash EEPROM Devices Via the Addition of a Shallow Source Side Implanted Region," discloses a process for fabricating a flash EEPROM device.

U.S. Patent 6,380,583 to Hsieh et al., "Method to Increase Coupling Ratio of Source to Floating Gate in Split-Gate Flash," discloses a split-gate flash memory cell having a three-dimensional source capable of three-dimensional coupling with the floating gate of the cell, as well as a method of forming the same.

U.S. Patent 6,403,494 to Chu et al., "Method of Forming a Floating Gate Self-Aligned to STI on EEPROM," discloses a method for forming a split-gate flash memory cell where the floating gate of the cell is self-aligned to a shallow trench isolation (STI), which in turn makes it self-aligned to source and to word line.

U.S. Patent 6,326,660 to Lin et al., "Method to Improve the Capacity of Data Retention and Increase the Coupling Ratio of Source to Floating Gate in Split-Gate Flash," discloses a method for forming a split-gate flash memory cell having reduced size, increased capacitive coupling and improved data retention capability.

U.S. Patent 5,643,814 to Chung, "Method of Making an EEPROM with an Erase Gate," describes a method of making a split gate flash memory.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-02-353	10/661,746
Applicant: Chia-Ta Hsieh	
Filing Date: 09/12/03	Group Art Unit

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5915178	6/22/99	Chiang et al.	438	266	12/8/97
	6380583	4/30/02	Hsieh et al.	257	314	10/6/00
	6403494	6/11/02	Chu et al.	438	719	8/14/00
	6326660	12/4/01	Lin et al.	257	314	3/13/00
	5643814	7/1/97	Chung	437	43	12/7/95

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.